20. A circuit for connecting a memory device and a processing element of an active memory comprising:

a first multiplexer having a first input coupled to said processing element and a second input coupled to a data bus of said memory device;

a first register having an input and an output, said input being coupled to an output of said first multiplexer;

a second multiplexer having an input coupled to said output of said first register and an output coupled to said processing element;

a first tri-state device having an input coupled to said output of said first register and an output coupled to said data bus;

a second tri-state device having an input coupled to said output of said first register and an output coupled to said data bus and a third input of said first multiplexer;

a second register having an input coupled to said output of said first multiplexer;

a third multiplexer having a first input, a second input, and an output, said first input being connected to an output of said second register, said output from said first register being

coupled to said second input, said output being coupled to said input of said second multiplexer; and

a fourth multiplexer having a first input, a second input, and an output, said first input being coupled to said output of said first register, said second input being coupled to said output of said second register, said output being coupled to said input of said first and second tri-state devices.

41. A method for writing data from a processing element to a memory device comprising the steps of:

providing a plurality of data bits in a serial manner from said processing element to a data circuit;

passing said data through said data circuit; and

writing said data to said memory device,

wherein said data circuit passes said data directly to said memory device in a horizontal mode and

wherein said step of passing said data further comprises:

outputting each bit of said plurality of data bits from said data circuit on a different data bus associated with said memory device; and

wherein said step of writing said data further comprises writing said each bit of said plurality of bits data bits to a location in said memory device associated with a different address.

43. The method according to claim 41, wherein said step outputting further comprises:

passing each bit of said plurality of data bits through a respective register.

44. The method according to claim 41, wherein each different memory address has an associated plurality of bits, and wherein said step of writing each said data bit further comprises:

writing said each bit into a same bit of said associated plurality of bits in each said different memory address.

48. A method for reading data stored in a memory device and providing said data to a processing element, said method comprising the steps of:

providing a plurality of data bits from said memory device to a data circuit;

passing said data through said data circuit; and

outputting said data to said processing element in a serial manner, and

wherein at least a portion of said data is stored in said memory device in a vertical mode.

51. The method according to claim 48, wherein said step of passing said at least a portion of said data further comprises:

passing a respective bit of data associated with a different address through a respective register; and

inputting each said respective bit of data associated with said different address to a multiplexer,

wherein said multiplexer outputs said each said respective bit of data in a serial manner to said processing element.